

## Claims

What is claimed is:

- 5 1. A digital signaling system comprising:  
a transmit circuit, the transmit circuit comprising a transmit data input and a  
transmit data output, the transmit circuit producing an transmit data output signal at the  
transmit data output based on a transmit data input signal from the transmit data input  
when the transmit circuit is operating in a normal mode, the transmit circuit further  
10 comprising a transmit repeating pattern generator producing a repeating pattern signal,  
the transmit circuit producing the transmit data output signal at the transmit data output  
based on the repeating pattern signal when the transmit circuit is operating in a test mode;  
and  
a receive circuit, the receive circuit operably coupled to the transmit circuit and  
15 receiving the transmit data output signal from the transmit circuit at a receive data input,  
the receive circuit comprising a receive data output, the receive circuit producing a  
receive data output signal at the receive data output based on transmit data output signal  
when the receive circuit is operating in the normal mode, the receive circuit further  
comprising a receive repeating pattern generator producing the repeating pattern signal,  
20 the receive circuit producing a comparison signal based on comparison dependent on the  
transmit data output signal and the repeating pattern signal when the receive circuit is  
operating in the test mode.
2. The digital signaling system of claim 1 wherein the transmit repeating pattern  
25 generator comprises a transmit shift register and the receive repeating pattern generator  
comprises a receive shift register.
3. The digital signaling system of claim 2 wherein a transmit shift register output of  
the transmit shift register is coupled a transmit shift register input of the transmit shift  
30 register when the transmit circuit is operating in the test mode and a receive shift register

output of the receive shift register is coupled to a receive shift register input of the receive shift register when the receive circuit is operating in the test mode.

4. The digital signaling system of claim 2 wherein the transmit circuit further  
5 comprises a transmit linear feedback logic gate, wherein a first transmit shift register  
output of the transmit shift register is coupled a first transmit linear feedback logic input  
of the transmit linear feedback logic gate and wherein a second transmit shift register  
output of the transmit shift register is coupled a second transmit linear feedback logic  
input of the transmit linear feedback logic gate, the transmit linear feedback logic gate  
10 producing a transmit linear feedback logic gate output signal upon which a transmit shift  
register input signal at a transmit shift register input of the transmit shift register depends  
when the transmit circuit is operating in the test mode and wherein the receive circuit  
further comprises a receive linear feedback logic gate, wherein a first receive shift  
register output of the receive shift register is coupled to a first receive linear feedback  
15 logic input of the receive linear feedback logic gate and wherein a second receive linear  
feedback logic input of the receive linear feedback logic gate, the receive linear feedback  
logic gate producing a receive linear feedback logic gate output signal upon which a  
receive shift register input signal at a receive shift register input of the receive shift  
register depends when the receive circuit is operating in the test mode.

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5. The digital signaling system of claim 1 wherein the transmit repeating pattern  
generator comprises a transmit linear feedback shift register and the receive repeating  
pattern generator comprises a receive linear feedback shift register.

25 6. The digital signaling system of claim 1 wherein the transmit data output signal is  
capable of representing two bits of information simultaneously over a single conductor.

7. The digital signaling system of claim 1 wherein the transmit data output signal is  
communicated over a single conductor referenced to a ground voltage.

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8. The digital signaling system of claim 1 wherein the transmit data output signal is communicated as a differential signal over two conductors.

9. A method for evaluating a digital signaling system comprising the steps of:  
generating a transmit repeating pattern in a transmit circuit;  
transmitting the transmit repeating pattern to a receive circuit;  
generating a receive repeating pattern in the receive circuit; and  
5 comparing the transmit repeating pattern to the receive repeating pattern to obtain  
a comparison.

10. The method of claim 9 further comprising the steps of:  
adjusting a parameter affecting operation of the transmit circuit based on the  
10 comparison.

11. The method of claim 10 wherein the parameter is selected from a group consisting  
of an output current, a crosstalk cancellation coefficient, and a self-equalization  
coefficient.

12. The method of claim 9 wherein the step of generating a transmit repeating pattern  
in a transmit circuit comprises the step of:  
utilizing a shift register to generate the transmit repeating pattern.

13. The method of claim 12 wherein the step of utilizing a shift register to generate  
the transmit repeating pattern comprises the step of:  
utilizing a linear feedback shift register to generate the transmit repeating pattern.

14. The method of claim 9 wherein the step of transmitting the transmit repeating  
25 pattern to the receive circuit further comprises the step of:  
transmitting the transmit repeating pattern as a signal referenced to a ground.

15. The method of claim 9 wherein the step of transmitting the transmit repeating  
pattern to the receive circuit further comprises the step of:  
30 transmitting the transmit repeating pattern as a differential signal over a pair of  
conductors.

16. The method of claim 9 wherein the step of transmitting the transmit repeating pattern to the receive circuit further comprises the step of:

5 transmitting the transmit repeating pattern by encoding two bits of information on a single conductor simultaneously.

17. The method of claim 9 further comprising the step of:  
adjusting a receiver characteristic of the receive circuit.

10 18. The method of claim 17 wherein the receiver characteristic is selected from a group consisting of an receive circuit timing signal and a voltage reference.

15 19. The method of claim 17 further comprising the step of:  
determining boundary values of the receiver characteristic within which reliable operation of the system is provided.

20 20. The method of claim 19 further comprising the steps of:  
adjusting a parameter affecting operation of the transmit circuit based on the boundary values.

21. The method of claim 20 wherein the parameter is selected from a group consisting of an output current, a crosstalk cancellation coefficient, and a self-equalization coefficient.